ABSTRACT OF THE DISCLOSURE

A capacitor structure having a first level of electrically conductive parallel lines and at least a second level of electrically conductive parallel lines disposed over the lines in the first level, the lines of the first and second levels being arranged in vertical rows. A dielectric layer is disposed between the first and second levels of conductive lines. One or more vias connect the first and second level lines in each of the rows, thereby forming a parallel array of vertical capacitor plates. Electrically opposing nodes form the terminals of the capacitor. The parallel array of vertical capacitor plates are electrically connected to the nodes in an alternating manner so that the plates have alternating electrical polarities.